

### REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-18 are currently pending in the application; Claims 1, 3, and 13 having been amended by way of the present response.

In the outstanding Office Action, Claims 1 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Maeda et al. (Maeda). Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Maeda.

Applicant appreciates the Examiner's indication that Claims 2, 6-8, 10, 12, and 16-18 are allowed, as well as the indication that Claims 3-5 and 13-15 include allowable subject matter, and though objected to, would be allowable if rewritten in independent form.

Applicant has so rewritten Claims 3 and 13. Further, Claims 4 and 5 and Claims 14 and 15 depend from newly independent Claims 3 and 13, respectively. Thus, for these reasons, Applicant respectfully requests that the objection to Claims 3-5 and 13-15 be withdrawn and the claims allowed.

The present invention is directed to a semiconductor power amplifier. The power amplifier receives a high frequency signal inputted to a signal input terminal, amplifies the signal using first and second transistors connected in parallel, and outputs the amplified signal via a signal output terminal. The power amplifier includes a first capacitor element connected between the signal input terminal and an input terminal of the first transistor. A second capacitor is connected between the signal input terminal and an input terminal of the second transistor. One end of a first impedance element (e.g., a resistor) is directly connected to the input terminal of the first transistor, and the other end is directly connected to the input terminal of the second transistor (i.e., no other elements are disposed between the impedance

element and the inputs of the transistors).

Maeda shows a divider/combiner. As shown in figure 27, for example, of Maeda, as best understood by Applicant in view of the numerous typographical errors in the printed patent, a divider 2710 includes a phase shifter 2720. The phase shifter 2720 has a capacitor 2721, a resistor (i.e., impedance element) 2722, and a capacitor 2723 arranged in series and connected with FETs (i.e., transistors) 2240, 2244. As shown in the figures, the capacitors 2721, 2723, rather than the resistor 2722, are connected with the FETs (i.e., the capacitors 2721, 2723 are disposed between the impedance element 2722 and the transistors 2240, 2244).<sup>1</sup> Thus, for these reasons, Applicant respectfully asserts that Maeda does not show the claimed features of an impedance element connected to first and second transistors.

Specifically, independent Claim 1 recites "a first impedance element, one end of which is connected to the input terminal of said first transistor, and the other end of which is connected to the input terminal of said second transistor." In view of the above-discussion, Applicant respectfully requests that the rejection of independent Claim 1 under 35 U.S.C. § 102(b) be withdrawn and the claim allowed.

Claims 9 and 11 depend from independent Claim 1, and are therefore also allowable for at least the same reasons as the independent claim. Thus, for these reasons, Applicant respectfully requests that the rejections of dependent Claims 9 and 11 be withdrawn and the claims allowed.

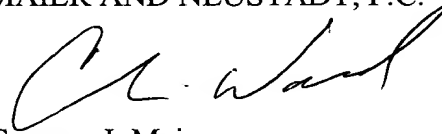
---

<sup>1</sup>From column 23, line 38 to column 24, line 15.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER AND NEUSTADT, P.C.



Gregory J. Maier  
Registration No. 25,599  
Attorney of Record  
Christopher D. Ward  
Registration No. 41,367



**22850**

GJM:CDW:PH:bwt  
I:\atty\PH\20s\205263\205263US2\_AM.wpd

**Marked-Up Copy**

Serial No: 09/817,216

Amendment Filed on:

6-28-02

IN THE CLAIMS

1. (Amended) A semiconductor power amplifier for amplifying a high frequency signal inputted to a signal input terminal by first and second transistors connected in parallel to each other to output the amplified signal via a signal output terminal, said semiconductor power amplifier comprising:

a first capacitor element connected between said signal input terminal and an input terminal of said first transistor;

a second capacitor element connected between said signal input terminal and an input terminal of said second transistor; and

a first impedance element, one end of which is connected to the input terminal of said first transistor, and the other end of which is connected to the input terminal of said second transistor [connected between the respective input terminals of said first and second transistors].

3. (Amended) A [The] semiconductor power amplifier [according to claim 1,] for amplifying a high frequency signal inputted to a signal input terminal by first and second transistors connected in parallel to each other to output the amplified signal via a signal output terminal, said semiconductor power amplifier [further] comprising:

a first capacitor element connected between said signal input terminal and an input

terminal of said first transistor;

a second capacitor element connected between said signal input terminal and an input terminal of said second transistor; and

a first impedance element, one end of which is connected to the input terminal of said first transistor, and the other end of which is connected to the input terminal of said second transistor,

a first power amplifying section comprising said first and second transistors, said first and second capacitor elements, and said first impedance element;

a second power amplifying section disposed separately from said first power amplifying section, said second power amplifying section including said first and second transistors, said first and second capacitor elements, and said first impedance element; and

a second impedance element connected between said first impedance element in said first power amplifying section and said first impedance element in said second power amplifying section,

wherein the respective input terminals of said first and second power amplifying sections are connected to said signal input terminal via the first and second inductor elements.

13. (Amended) A multistage monolithic integrated circuit comprising:

a plurality of amplifiers connected in cascade,

wherein a last-stage amplifier of these amplifiers [is constituted of the] includes a semiconductor power amplifier [according to claim 1] for amplifying a high frequency signal inputted to a signal input terminal by first and second transistors connected in parallel to each other to output the amplified signal via a signal output terminal, said semiconductor power amplifier comprising:

a first capacitor element connected between said signal input terminal and an input terminal of said first transistor;

a second capacitor element connected between said signal input terminal and an input terminal of said second transistor; and

a first impedance element, one end of which is connected to the input terminal of said first transistor, and the other end of which is connected to the input terminal of said second transistor.